CLAIMS

What is claimed is:

1. A memory device, comprising:

an address bus interface;

an address bus termination circuit that can be enabled or disabled; and

an address bus termination control signal input.

2. The memory device of claim 1, the address bus termination circuit to be enabled if an asserted address bus termination control signal is received at the address bus termination control signal input.

3. The memory device of claim 2, the address bus termination circuit to be disabled if the address bus termination control signal is not asserted.

4. The memory device of claim 3, wherein the address bus termination control signal is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level.

5. The memory device of claim 3, wherein the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level.

6. The memory device of claim 3, further comprising a data bus interface and a data bus termination circuit.

7. The memory device of claim 6, further comprising a data bus termination control signal input, the data bus termination circuit to be enabled in response to an asserted data bus termination control signal.

8. A memory module, comprising:

a plurality of memory devices coupled to an address bus in a daisy chain configuration, each of the plurality of memory devices including

an address bus interface,

an address bus termination circuit that can be enabled or disabled, and

an address bus termination control signal input.

9. The memory module of claim 8, wherein for each of the plurality of memory devices the address bus termination circuit is enabled if an asserted address bus termination control signal is received at the address bus termination control signal input.

10. The memory module of claim 9, wherein for each of the plurality of memory devices the address bus termination circuit is disabled if the address bus termination control signal is not asserted.

11. The memory module of claim 10, wherein for each of the plurality of memory devices the address bus termination control signal is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level.

12. The memory module of claim 11, wherein all but the last memory device in the daisy chain configuration has its address bus termination control signal input tied to ground and the last memory device in the daisy chain configuration has its address bus termination control signal tied to a positive voltage.

13. The memory module of claim 10, wherein for each of the plurality of memory devices the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level.

14. The memory module of claim 13, wherein all but the last memory device in the daisy chain configuration has its address bus termination control signal input tied to a positive voltage and the last memory device in the daisy chain configuration has its address bus termination control signal tied to ground.

15. The memory module of claim 10, wherein each of the plurality of memory devices further includes a data bus interface and a data bus termination circuit.

16. The memory module of claim 15, wherein each of the plurality of memory devices further includes a data bus termination control signal input, the data bus termination circuit to be enabled in response to an asserted data bus termination control signal.

17. A method, comprising:

connecting in a daisy chain configuration an address bus to a plurality of memory devices on a memory module;

providing address bus termination circuitry in the plurality of memory devices; and

enabling the address bus termination circuitry of only one of the plurality of memory devices.

18. The method of claim 17, wherein enabling the address bus termination circuitry of only one of the plurality of memory devices includes enabling the address bus termination circuitry of the last memory device in the daisy chain configuration.

19. The method of claim 18, wherein enabling the last memory device in the daisy chain configuration includes coupling an address bus termination control pin to a positive voltage.

20. The method of claim 19, wherein enabling the address bus termination circuitry of only one of the plurality of memory devices includes disabling the address bus termination circuits in all but the last memory device in the daisy chain configuration by coupling address bus termination control pins on all but the last memory device to ground.